CLAIM REVISIONS

1. (previously presented) A signal router, comprising:

a conditioning circuit configured to write K identical images of a first set of data from N inputs to K random access memories during a first time interval;

K respective bit selectors each configured to read respective portions of a respective one of said K identical images;

said K respective bit selectors being coupled to construct M output data streams during a second time interval

wherein each of the random access memories comprises exactly two parts configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts.

2. (canceled)

3. (previously presented) A signal router, as in claim 1, wherein said conditioning circuit includes a buss to which said first set of data is applied and addressing controllers configured to write data from said buss to said random access memories, whereby said K identical images are written.

4. (previously presented) A signal router, comprising:

a controller programmed to store identical images of data from said N inputs in K memories;

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said controller being further programmed to read respective bits of said data from each of said K memories to produce M respective output data streams, whereby N inputs are mapped to M outputs,

wherein each of the K memories comprises exactly two parts configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts.

5. (currently amended) A router as in claim 4, further comprising a data buss connected to receive said N inputs and distribute them to said K memories, wherein pre-sorting of the input data is not necessary.

6. (currently amended) A router as in claim 5, wherein a bit rate of each of said ~~K~~ M output streams is less than a bit rate of said buss.

7. (previously presented) A method of routing data from N inputs to M outputs, comprising the steps of:

applying data from said N inputs to a data buss by means of at least one of time and space multiplexing;

imaging said data on K random access memories from said buss;

reading respective sets of bits from said random access memories to form respective ones of said signals ultimately demultiplexed to form said M outputs,

wherein each of the random access memories comprises exactly two parts configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts.

8. (previously presented) The router of claim 1, wherein the parts are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read.

9. (previously presented) The router of claim 4, wherein the parts are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read.

10. (previously presented) The method of claim 7, wherein the parts are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read.

11. (currently amended) A signal router, comprising:

- N inputs for receiving synchronous streams of serial broadcast data;
- a conditioning circuit configured to write K identical images of a first set of data from the N inputs to K memories during a first time interval;
- K respective bit selectors each configured to read respective portions of a respective one of said K identical images; and
- each of said K respective bit selectors being coupled to construct M output data streams during a second time interval.